REMARKS

The Applicant is filing a continuation pursuant to 37 C.F.R. § 1.53(b) to continue the prosecution of the parent case of this Application. In the parent case, an Office Action was issued on June 4, 2003. In response to that Office Action, the Applicant filed an Amendment and Response to place the claims that were objected to in condition for allowance. In this continuation, the Applicant is canceling claims 11, 17, 24 and 25 because those claims were ultimately allowed in the parent case. Accordingly, claims 11, 17, 24 and 25 are not discussed further herein. Claims 1, 12 and 30 are currently amended to correct minor informalities in their presentation and new claims 32 and 33 have been added. Thus, claims 1-10, 12-16, 18-23 and 26-33 are pending in the Application.

In the June 4, 2003 Office Action in the parent case, the Examiner objected to the Specification for informalities in the Cross Reference to Related Application. The missing information has been added to the present case in this Preliminary Amendment.

In the Office Action, claims 1-4, 7, 9, 10, 12, 13, 15, 16, 18-23 and 26-31 were rejected under 35 U.S.C. § 103(a) as being obvious based on U.S. Patent No. 6,457,100 to Ignatowski et al. ("the Ignatowski reference") in view of U.S. Patent No. 5,440,752 to Lentz ("the Lentz reference"). Claims 5, 6 and 14 were rejected under 35 U.S.C. § 103(a) as being obvious based on Ignatowski in view of Lentz and further in view of U.S. Patent No. 6,202,127 to Dean et al. ("the Dean reference"). Additionally, claim 8 was rejected under 35 U.S.C. § 103(a) as being obvious based on Ignatowski in view of Lentz and further in view of U.S. Patent No. 5,467,679 to Eng et al. ("the Eng reference"). Each of these rejections is addressed in detail below.

The Rejections Under 35 U.S.C. § 103

As set forth above, claims 1-4, 7, 9, 10, 12, 13, 15, 16, 18-23 and 26-31 were rejected as obvious under Section 103 based on Ignatowski in view of Lentz. Claims 5, 6 and 14 were rejected under Section 103 based on Ignatowski in view of Lentz and further in view of Dean. Claim 8 was rejected under Section 103 based on Ignatowski in view of Lentz and further in view of Eng. With respect to claims 1-4, 7, 9, 10, 12, 13, 15, 16, 18-23 and 26-31, the Examiner stated:

> 6. Claims 1-4, 7, 9-10, 12-13, 15-16, 18-23 and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ignatowski et al. (US PAT. 6,457,100 hereinafter Ignatowski) in view of Lentz et al. (US PAT. 5,440,752 hereinafter Lentz).
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> Regarding claim 1, Ignatowski discloses a chip-multiprocessing system with scalable architecture (41, figure 3), comprising on a single chip, a plurality of processor cores (15-1 - 15-N, figure 3), a two level cache hierarchy including a first level caches as private cache for each related processor (col. 8 lines 24-35), a second level cache with a relaxed inclusion property (40, figure 3), the second-level cache, i.e., common cache (40, figure 3) being logically shared by the plurality of processor cores (col. 9 lines 8-10), the second level cache being modular with a plurality of interleaved modules (col. 16 lines 33-40 and col. 18 lines 40-46), one or more memory controllers (4, figure 1) capable of operatively communicating with the two-level cache hierarchy and with an off-chip memory (col. 4 line 58 through col. 7 line 24), a cache coherence protocol, one or more coherence protocol engines, i.e., nodal directory, (col. 9 line 64 through col. 10 line 24), an intra-chip switch, i.e., an electronic cross point-type switch, and interconnect subsystem, i.e., inter-node bus. Although Ignatowski differs from the claimed invention in not specifically teaches the first level caches comprising a pair of instruction and data caches. It is well known in the art that the first level cache comprising both data and instruction caches for faster execute and access by the central processor, as an example of Lentz teaches in the multiple processing system (1, figure 1), each processors comprising a data cache 51 and an instruction cache 52 (figure 2 and col. 6 line 65 through col. 7 line 19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple processing system of Ignatowski in having a pair of data and instruction

cache as the first level cache, as per teach of Lentz because it reduces the latency of memory accesses and speed up an access by any processor with their private data and instruction caches.

Regarding claim 2, Ignatowski discloses a chip-multiprocessing system wherein the scalable architecture is targeted at parallel commercial workloads (col. 4 line 58 through col. 7 line 8).

Regarding claim 3, Ignatowski discloses a chip-multiprocessing system further comprising on a single I/O chip, a processor core similar in structure and function to the plurality of processor cores (col. 8 lines 23-35), a single-module second level cache (40, figure 3) with controller (27, figure 3), an I/O router (col. 12 line 52 col. 3 line 7), and a memory that participates in the cache coherency protocol (28-1 - 28-M, figure 3 and col. 15 line 48 through col. 16 line 9).

Regarding claim 4, Ignatowski discloses a chip-multiprocessing system wherein the plurality of core processors are each a single-issue, in-order processor configured with a pipelined data path and hardware support for floating-point operations (col. 4 line 58 through col. 7 line 8).

Regarding claim 7, Lentz discloses a chip-multiprocessing system wherein each of the plurality of processor cores is capable of separately interfacing (55 and 56, figure 2) with either of the instruction and data caches, and wherein each of the caches is configured for single-cycle latency (col. 7 line 29 through col. 8 line 14).

Regarding claim 9, Ignatowski discloses a chip-multiprocessing system wherein the single chip creates a node, and wherein the coherence protocol engines include a home engine and a remote engine which support shared memory across multiple nodes (col. 9 line 26 through col. 10 line 35).

Regarding claim 10, Ignatowski discloses a chip-multiprocessing system further comprising a system control module that takes care of system initialization and maintenance including configuration, interrupt handling, and performance monitoring (col. 4 line 58 through col. 7 line 8).

Regarding claim 12, Ignatowski discloses a chip-multiprocessing system wherein each bank of memory chips includes DRAM (col. 15 lines 5-24).

Regarding claim 13, the difference between Lentz and the claims is the claims specifically recite the second level

cache is interleaved into eight modules. However, having this sized memory does not have a disclosed purpose nor is this size disclosed to overcome any deficiencies in the prior art. As such, the memory may have been of any size. In addition, since Lentz teaches the cache is able to program and interleave (col. 7 lines 3-28), the ordinary artisan would realize a possible memory size increase, as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the system of Lentz wherein the cache is interleaved into vary size, as disclosed supra, since applicant has not disclosed that an interleaved eight modules, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose.

Regarding claim 15, Lentz discloses a chip-multiprocessing system wherein each instruction cache is kept coherent by hardware (col. 7 lines 3-19).

Regarding claim 16, Ignatowski discloses a chip-multiprocessing system wherein each of the second level cache modules includes an N-way set associative cache and use a round-robin or least-recently-loaded replacement policy if an invalid block is not available (col. 9 lines 8-24).

Regarding claim 18, Ignatowski discloses a chip-multiprocessing system wherein the pair of instruction and data caches includes a first state field per each cache line present therein the first state field having bits related to the MESI (col. 14 lines 33-41 and col. 16 lines 41-55).

Regarding claims 19-20, Ignatowski discloses a chip-multiprocessing system wherein the second level cache maintains a duplicate of the first state fields from the first-level cache pairs of instructions and data caches, the duplicate being maintained in order to avoid the need for a first-level cache lookup for cache lines that map to given addresses of corresponding requested cache lines and the second level cache holds a second state field for each cache line present therein, the second state field having bits related to the MESI protocol, wherein the second level cache maintains a duplicate of the first state field, and wherein on every second level cache access the duplicate first state fields and the second state fields are accessed in parallel (col. 16 line 41 through col. 17 line 12 and col. 17 line 56 through col. 18 line 28).

Regarding claim 21, Ignatowski discloses a chip-multiprocessing system wherein the single chip creates a node (41-1 - 41-4, figure 4), and wherein information about sharing of data across nodes in kept in a directory in a memory accessed

via the memory controllers (col. 18 line 47 through col. 19 line 26).

Regarding claim 22, Ignatowski discloses a chip-multiprocessing system wherein the second level cache includes a controller (27, figure 3), and wherein manipulation and interpretation of the directory is done by the protocol engines, although the controller also interprets the directory, but merely for determining whether a cache line is cached remotely to the single chip (col. 15 line 48 through col. 16 line 40).

Regarding claim 23, Ignatowski discloses a chip-multiprocessing system wherein the interconnect subsystem includes at least one data path (33A and 33B, figure 5), and wherein the interconnect subsystem is a crossbar configured with a uni-directional, push-only interface, and is capable of scheduling data transfers according to data paths availability, pre-allocating data paths, speculatively asserting a requester's grant single, and supporting back-to-back transfer without dead-cycles between transfers (col. 21 line 60 through col. 22 line 8).

Regarding claim 26, Ignatowski discloses a chip-multiprocessing system wherein the memory controller includes a memory access controller with high-speed interface circuitry and a memory controller engine capable of scheduling second-level cache memory access (col. 15 line 48 through col. 16 line 32).

Regarding claim 27, Ignatowski discloses a chip-multiprocessing system wherein the coherence protocol engines are implemented as similarly structured micro-programmable controllers, although each of them as its respective micro-code (col. 16 line 41 through col. 17 line 19).

Regarding claim 28, Ignatowski discloses a chip-multiprocessing system wherein each of the coherence protocol engines is corresponding to determine the requested data and/or instruction in the coherence protocol (MESI). Although Ignatowski failed to clearly discloses the coherence protocol engines is configured with an input state, a microcode-controlled execution stage and an output stage. It recognizes that a step of a requested data from processor to compare the status in the coherence protocol engines as an input stage, a step of determine the status of requested data by MESI protocol as a microcode-controlled execution stage, and a step of output the status of the requested data as an output stage (col. 17 line 56 through col. 19 line 1).

Regarding claim 29, the difference between Ignatowski and the claims is the claims specifically recite the protocol code that includes instructions named Send, Receive, Lsend, Lreceive, Test, Set and Move. However, having the special instruction name does not have a disclosed purpose nor is this names disclosed to overcome any deficiencies in the prior art. As such, the instruction name may have been of vary name. In addition, since Ignatowski discloses the directory information (hit, miss, exclusive, modified, invalid, etc...) at col. 17 lines 13-19. Accordingly, it would have been an obvious matter of design choice to utilize the system of Ignatowski wherein the protocol code (hit, miss, exclusive, modified, invalid, etc...), as disclosed supra, since applicant has not disclosed that the instructions named Send, Receive, Lsend, Lreceive, Test, Set and Move, as opposed to other names, overcomes a deficiency in the prior art or it for any stated purpose.

Regarding claim 30, Regarding claim 1, Ignatowski discloses a chip-multiprocessing system with scalable architecture (41, figure 3), comprising on a single chip, a plurality of processor cores (15-1 - 15-N, figure 3), a two level cache hierarchy including a first level caches as private cache for each related processor (col. 8 lines 24-35), a second level cache with a relaxed inclusion property (40, figure 3), the second-level cache, i.e., common cache (40, figure 3) being logically shared by the plurality of processor cares (col. 9 lines 8-10), the second level cache being modular with a plurality of interleaved modules (col. 16 lines 33-40 and col. 18 lines 40-46), one or more memory controllers (4, figure 1) capable of operatively communicating with the two-level cache hierarchy and with an off-chip memory (col. 4 line 58 through col. 7 line 24), a cache coherence protocol, one or more coherence protocol engines, i.e., nodal directory, (col. 9 line 64 through col. 10 line 24), an intra-chip switch, i.e., an electronic cross point-type switch, and interconnect subsystem, i.e., inter-node bus, the single chip creates a node (41-1 - 41-4, figure 5) and providing one ore more than one of the nodes to create in a modular scalable fashion, a glueless multiprocessor (col. 22 line 18-63). Although Ignatowski differs from the claimed invention in not specifically teaches the first level caches comprising a pair of instruction and data caches. It is well known in the art that the first level cache comprising both data and instruction caches for faster execute and access by the central processor, as an example of Lentz teaches in the multiple processing system (1, figure 1), each processors comprising a data cache 51 and an instruction cache 52 (figure 2 and col. 6 line 65 through col. 7 line 19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple processing

system of Ignatowski in having a pair of data and instruction cache as the first level cache, as per teach of Lentz because it reduces the latency of memory accesses and speed up an access by any processor with their private data and instruction caches.

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Office Action, pages 3-10.

With respect to claims 5, 6 and 14, the Examiner stated:

7. Claims 5-6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ignatowski et al. (US PAT. 6,457,100 hereinafter Ignatowski) and Lentz et al. (US PAT. 5,440,752 hereinafter Lentz) as applied to claim 1 above, and further in view of Dean et al. (US PAT. 6,202,127 hereinafter Dean).

Regarding claims 5-6, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein the plurality of processor cores are each capable of executing an instructions set of the ALPHA™ processing core and each configured with a branch target buffer, pre-compute logic for ranch conditions, and a fully bypassed data path. However Dean teaches such (col. 2 lines 61-65 and col. 3 line 56 through col. 3 line 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having the plurality of processor cores are each capable of executing an instructions set of the ALPHA™ processing core and each configured with a branch target buffer, pre-compute logic for ranch conditions, and a fully bypassed data path, as per teaching of Dean, because it implements the chip-multiprocessing system and reduces memory latency.

Regarding claim 14, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein each of the instruction and data caches is a two-way set-associative cache with virtual indices and physical tags. However Dean teaches such (col. 3 line 20 through col. 4 line 21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having each of the instruction and data caches is a two-way set-associative cache with virtual indices

and physical tags, as per teaching of Dean, because it implements the chip-multiprocessing system and reduces memory latency.

Office Action, pages 10-11.

With respect to claim 8, the Examiner stated:

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ignatowski et al. (US PAT. 6,457,100 hereinafter Ignatowski) and Lentz et al. (US PAT. 5,440,752 hereinafter Lentz) as applied to claim 1 above, and further in view of Eng et al. (US PAT. 5,467,679 hereinafter Eng).

Regarding claim 8, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein the interconnect subsystem includes a network router, a packet switch and input and output queues. However, Eng teaches such (col. 4 line 41 through col. 5 line 31). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having the interconnect subsystem includes a network router, a packet switch and input and output queues, as per teaching of Eng, because it reduces buffer space and increase throughput is achieved by providing shared memory.

Office Action, page 11.

The Applicant respectfully traverses these rejections. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would

have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

In the present case, the combination of Ignatowski and Lentz cannot render the Applicant's claims obvious under Section 103 because that combination does not include all of the elements recited in the Applicant's claims. Specifically, independent claim 1 requires "[a] chip-multiprocessing system with scalable architecture, comprising *on a single chip. . .*" a plurality of additional elements having the relationship set forth in the claim. (Emphasis added). One of the additional elements set forth in claim 1 is "a second level cache *with a relaxed inclusion property.*" (Emphasis added). Independent method claim 30 contains analogous limitations.

The Examiner incorrectly asserts that the device disclosed in Ignatowski is disposed on a single chip. In fact, the processor cores disclosed in Ignatowski are all on separate chips. Ignatowski clearly states that:

> FIG. 3 illustrates a node containing "N" *of the processor chips and memory combinations 15 shown in FIG. 1*, in which a bus interface unit 13 is connected to a bidirectional intra-node data bus 20 which connects to one end of a set of bidirectional buses of which each bus has its other end connected to a different nodal section chip 28, through an electronic section switch 22.
>
> Ignatowski, col. 13, lines 55-61 (Emphasis added).

The technologies involved in connecting functional units within an integrated circuit device are significantly different than the technologies that are employed to connect different integrated circuit devices together. Accordingly, the Applicant respectfully asserts that the Ignatowski reference does not teach, suggest or illustrate the disposition of the elements recited in independent claims 1 and 30 on a single integrated circuit device.

In addition to the failure of Ignatowski to disclose the elements of independent claims 1 and 30 disposed on a singe integrated circuit chip, Ignatowski fails to disclose a second level cache with a relaxed inclusion property. This point is not even subject to argument because the Ignatowski reference contains no occurrence of either the word "inclusion" or the word "property."

The Lentz reference, which the Examiner combined with Ignatowski to reject the Applicant's independent claims, does not supply the elements that are missing from Ignatowski. Specifically, the Lentz reference does not teach, suggest or illustrate the disposition of the elements recited in the Applicant's independent claims on a single chip.

The Lentz reference also fails to teach, suggest or illustrate the desirability of employing a second level cache with a relaxed inclusion property. Like Ignatowski, Lentz contains neither the term "inclusion" nor the term "property." Accordingly, no combination of Ignatowski and Lentz can render obvious independent claims 1 and 30 or the claims dependent thereon.

For at least these reasons, the combination of Ignatowski and Lentz fails to meet the limitations of independent claims 1 and 30. Thus, the Applicant respectfully requests that the rejection of claims 1 and 30 and the claims dependent thereon based on Ignatowski in view of Lentz not be repeated.

As set forth above, claims 5, 6, 8 and 14 were rejected under Section 103 based on Ignatowski in view of Lentz and further in view of either Dean or Eng. The Applicant respectfully asserts that the rejections of claims 5, 6, 8 and 14 are defective for at least the reasons set forth above with respect to independent claims 1 and 30. The Dean and Eng references are relied on by the Examiner only to show the omission of minor elements of dependent claims. For example, Dean is used by the Examiner to show a two-way set-associative cache with virtual indices and physical tags. Eng is used to show a system that includes a network router, a packet switch and input/output queues. Neither Dean nor Eng is asserted by the Examiner to disclose the elements set forth in claims 1 and 30 on a single integrated circuit device. Similarly, neither Dean nor Eng is asserted by the Examiner to disclose a second level cache with a relaxed inclusion property. Accordingly, the Applicant respectfully asserts that the addition of Dean or Eng to the combination of Ignatowski and Lentz cannot render the Applicant's claims obvious. The Applicant respectfully requests that the rejections of claims 5, 6, 8 and 14 under Section 103 based on Ignatowski in view of Lentz and further in view of either Dean or Eng not be repeated.

New Claims 32 and 33

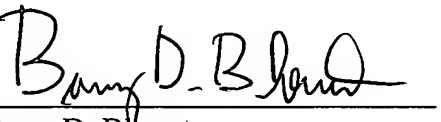
As set forth above, new claims 32 and 33 are presented herein for the first time. The Applicant respectfully asserts that new claims 32 and 33 are allowable over the prior art of record. An indication of the allowability of new claims 32 and 33 is, accordingly, respectfully requested.

Conclusion

In view of the amendments and remarks set forth above, the Applicant respectfully requests that the Examiner not repeat the rejections made during prosecution of the parent case to this Application. Furthermore, the Applicant asserts that an indication of the allowability of claims 1-10, 12-16, 18-23 and 26-33 is appropriate. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: October 24, 2003



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